

**TITLE: A DIRECT CONVERSION RF TRANSCEIVER  
FOR WIRELESS COMMUNICATIONS**

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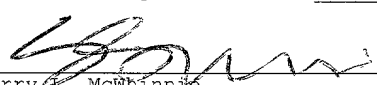
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**SPECIFICATION**  
**BACKGROUND**

**1. Technical Field**

5 The present invention relates to wireless communications and, more particularly, wideband wireless communication systems.

**2. Related Art**

Super-heterodyne receivers traditionally receive an RF signal that must be converted to base band by way of an intermediate  
10 frequency (IF). Thereafter, the IF signal is amplified and filtered to define a communication channel. In a transmitter, similarly, a base band signal is up converted to the intermediate frequency wherein the amplification and subsequent filtering are carried out at the IF stages. While  
15 some systems skip the IF conversion step, wideband systems typically require conversion to IF stages. Depending on the signal bandwidth and the type of communication system, semiconductor devices are not yet able to allow full integration of active filters operating at the elevated  
20 intermediate frequencies for a wideband or high data rate communication network. To carry out filtering at the intermediate frequencies, surface acoustic wave filters (SAW) are commonly used. The SAW filters have the drawback, however, of being bulky, heavy and expensive. Additionally,  
25 the SAW filters require low impedance matching thereby

resulting in high power consumption. Because they are often powered by battery, portable wireless communication devices are not readily adaptable for such systems in that they are required to be inexpensive, light and consume lower amounts of power. Thus, there is a need to design transceiver systems that eliminate the use of intermediate frequency filters.

An alternate approach to using a higher intermediate frequency that requires the SAW filters is to convert the RF signal to an intermediate frequency that is sufficiently low to allow the integration of on-chip channel selection filters. For example, some narrow band or low data rate systems, such as Bluetooth, use this low intermediate frequency design approach.

One problem using low intermediate frequencies, however, is satisfying image rejection requirements for the systems. The image rejection requirement for the down conversion is hard to meet and is usually limited to about -40 dB. Thus, this low intermediate frequency approach is limited for narrow band or low data rate systems. Wide band or high data rate systems require an intermediate frequency that is not low enough for the integration of channel selection filters given the technology that is available today for semiconductor processes. There is a need, therefore, for a wireless

transceiver system that allows for full integration on-chip of circuit designs that support high data rate and wideband communications.

**SUMMARY OF THE INVENTION**

A single chip radio transceiver includes circuitry that enables received wideband RF signals to be down converted to base band frequencies and base band signals to be up converted to wideband RF signals prior to transmission without requiring conversion to an intermediate frequency. Accordingly, image rejection problems are not encountered. Because of the present design, there further is no need to utilize large, expensive and heavy SAW filters as a part of the signal processing.

More specifically, a received RF signal is amplified by a low noise amplifier and then is mixed with a local oscillation (LO) signal having frequency that is correctly located at the frequency of received RF signal with automatic frequency control circuitry. Additionally, a plurality of filters are used to filter out low frequency interference including  $1/f$  interference and DC offset signals and to filter out high frequency interference.

Additionally, a plurality of received signal strength indication (RSSI) circuits are used to measure the power of the received signal as well as the power of the received signal with wide band interference. According to a ratio of the two measurements frontal and rear stage amplification values are affected in an inverse proportional manner. In the described invention, the frontal stage includes a low noise amplifier and

a high pass variable gain amplifier. The rear stage includes two additional high pass variable gain amplifiers. Thus, in the described embodiment, the gain of the first two amplifiers is adjusted in an inversely proportional manner to the rear stage amplifiers such that the total gain level remains constant. The receiver, therefore, has highest overall linearity.

Other aspects of the present invention will become apparent with further reference to the drawings and specification, which follow.

**BRIEF DESCRIPTION OF THE DRAWINGS**

A better understanding of the present invention can be obtained when the following detailed description of the preferred embodiment is considered with the following  
5 drawings, in which:

Figures 1A, 1B, 1C and 1D are frequency response curves and Figure 1E is a block diagram that illustrate some of the challenges that exist for developing zero IF systems that are all integrated within a semiconductor device;

Figures 2A and 2B illustrate frequency response curves that are realized by the present inventive system or transceiver;

Figure 3 is a flowchart illustrating an overall method performed by the inventive transceiver according to one  
15 embodiment of the present invention;

Figure 4 is a flowchart that illustrates a method for adjusting the channel frequency to a desired channel frequency according to one embodiment of the present invention;

Figure 5 is a flowchart that illustrates a method for  
20 amplifying a received signal in a transceiver according to one embodiment of the present invention; and

Figure 6 is a functional block diagram of a transceiver formed according to one embodiment of the present invention.

**DETAILED DESCRIPTION OF THE DRAWINGS**

Generally, the present invention provides a transceiver that allows for wideband systems formed on a chip that allow for up and down converting from base band and radio frequency without  
5 conversion to an intermediate frequency (zero IF).

Figures 1A, 1B, 1C and 1D are frequency response curves that illustrate some of the challenges that exist for developing zero IF systems that are all integrated within a semiconductor device. Referring now to Figure 1A, a signal is transmitted over a wireless medium as an RF signal shown generally at 104. For processing by a receiver, however, that signal is first down converted to an intermediate frequency (IF) shown generally at 108, wherein some preliminary processing occurs. Thereafter, the signal is down converted  
10 from intermediate frequency 108 to base band frequency 112.

The foregoing discussion about SAW filters may be considered in view of the frequency shown generally at 116. If the intermediate frequency is low enough, then the filters may be developed on chip. As described previously, however,  
15 the image rejection of the on chip filters is not always satisfactory. Thus, it is desirable to develop a zero IF system, meaning that no intermediate frequencies are used, as is illustrated in Figure 1B, in order to satisfy image rejection requirements. Accordingly, received signals are



transmitted directly from the RF signal 104 to the base band frequency 112 as is shown in Figure 1B. Similarly, signals that are to be transmitted are up converted from base band frequency 112 to RF signal 104.

5 One problem with down converting signals directly from RF signal 104 to base band frequency 112 is that the process of down converting the signal immediately results in a DC offset 120, as is shown in Figure 1C. Additionally, a noise component, often described as a  $1/f$  interference, is illustrated in Figure 1D. As may be seen, the  $1/f$  interference is very high at low frequencies but tapers off as the frequency is increased. One problem with the DC offset and the  $1/f$  interference is that any amplification of the received signal includes amplification of interference and/or DC power from the DC offset thereby saturating the amplifier with signals other than the received or target signal.

10  
15  
20 Figure 1E further illustrates the process that generates most of the DC offset. For example, a local oscillator (LO) 130 often produces leakage current that is conducted into the input of an amplifier or a mixer. More specifically, as may be seen in Figure 1E, a local oscillator 130 has leakage current that is conducted into the input of low noise amplifier (LNA) 134 and the input of mixer 138. This type of self mixing produces the most of DC offset at the output of

the mixer 138. It is very important, therefore, to eliminate these leakage currents so that the DC offset is at a minimum level.

Figures 2A and 2B illustrate frequency response curves that are realized by the present inventive system or transceiver. Referring now to Figure 2A, a DC offset is shown at 204, while the low end of a received signal frequency is shown at 208. Figure 2B illustrates a high pass (HP) filter 220 that eliminates the DC-offset 204 and a low pass (LP) filter 214 that selects the desired signal channel by attenuating higher frequency interference. In reality, with limited accuracy of local oscillation frequency due to cheap reference crystal is used, if received signal could be down converted too low that it could be attenuated by the HP filter 220. And it could be down converted too high that is could be attenuated by the LP filter 214. In order to avoid signal degradation, automatic frequency control (AFC) is proposed as show in Figure 2A. Accordingly, the invention includes a transceiver that determines the difference between frequency 208 and ideal frequency 212 (as shown in Figure 2B) and adjusts LO frequency so that the low end of the received signal is located at 212 and the high end of the signal is located at 216.

Figure 2B illustrates that the down converted signal after LO frequency correction is located in the desired frequency range, wherein the low end of the frequency is at 212 and the high end is at 216. As may be seen, the channel for the received signal now ranges from the frequency shown at 212 to the frequency shown at 216. Moreover, Figure 2B shows a high pass filter frequency response curve 220. As may be seen, the channel of the received signal is well beyond the attenuation part of HP filter curve 220. Without adjusting the frequency of LO, the high pass filter, whose frequency response curve is shown in Figure 2B, would have filtered or eliminated some of the received signal thereby losing information. Thus, Figures 2A and 2B suggest that the inventive system includes circuitry for not only correcting LO frequency, but also to filter the received signal thereafter with a high pass filter and a low pass filter.

Figure 3 is a flowchart that illustrates an overall method performed by the inventive transceiver according to one embodiment of the present invention. Referring now to Figure 3, a first process step taken by the transceiver is to amplify a received RF signal with a low noise amplifier (step 304). Thereafter, the frequency of the received signal is adjusted by LO frequency with an automatic frequency control circuitry. In the described embodiment, a coarse adjustment

is made (step 308), as well as a fine adjustment that is made in the digital domain (step 312). Thereafter, the signal is down converted from a specified RF channel to a specified base band channel (step 316) and a low pass filter is applied to eliminate interference occurring above the channel (step 320). Thereafter, a DC offset and low frequency interference (e.g.,  $1/f$ ) is removed with at least one high pass filter tuned to pass the base band channel (step 324). Finally, the signals are amplified by a plurality of amplifiers. The amplification level of the amplifiers is adjusted in an inverse proportional manner according to interference levels so that total amplification remains constant (step 328).

Figure 4 is a flowchart that illustrates a method for adjusting the channel frequency to a desired channel frequency according to one embodiment of the present invention. Referring now to Figure 4, the inventive method includes initially measuring a center frequency for the received RF signal and determining the difference between that center frequency and the center frequency of a specified RF channel (step 404). Initially, a coarse difference is measured and is corrected by adjusting LO frequency. Then, the residual difference is adjusted to a fine degree of measurement in the digital domain to obtain an accurate difference between an actual center frequency and a specified center frequency (step

408). The difference in center frequencies is then transmitted to a signal generator (step 412). In the described embodiment of the invention, the signal generator for the transceiver is one that is capable of performing  
5 quadrature phase shift keyed modulation of signals. Accordingly, the difference in center frequency values determined in step 404 is transmitted to a sine and a cosine element of an encoder or signal generator.

After the difference in frequency has been sent to the  
10 sine/cosine encoders, the signals are transmitted from the encoders to a digital-to-analog converter (step 416). Thereafter, the digital-to-analog converter transmits the signals to a low pass filter to remove high frequency interference (step 420). Thereafter, the signal is  
15 transmitted to a mixer to produce a new local oscillator signal output. The new local oscillator output signal is characterized by the desired frequency channel (step 424).

Figure 5 is a flowchart that illustrates a method for  
20 amplifying a received signal in a transceiver according to one embodiment of the present invention. The method of Figure 5 generally includes using a plurality of received signal strength indicators (RSSI) to sense the power of the received interference and signal to determine a right amplification of cascaded amplifier stages. Initially, a first RSSI is used to

5 sense the power of the received interference and signal (step 504). Thereafter, a second RSSI is used to sense the power of the signal without the interference (step 508). After measuring the power of the signal, as well as the power of the interference and signal, the transceiver evaluates the ratio of signal power to signal and interference power to determine optimal amplification techniques by each of a plurality of amplifiers (step 512). If the interference level is high, the gain of a first amplifier is set to a lower value and the rear gain of a second amplifier, which is located after channel selection filter, is set to a higher value in a multi-amplifier system (step 516). If the interference value is relatively low, the frontal gain is set to a higher value and the rear gain is set to a lower value (step 520). As the gain of the frontal and rear amplifiers are adjusted, they are adjusted in a manner wherein the total amplification is kept at a constant level required for certain power level of desired channel or signal (step 524). In the described embodiment, an LNA is used for the front end and three high pass variable gain amplifiers (HP-VGA's) are used in subsequent stages.

Figure 6 is a functional block diagram of a transceiver formed according to one embodiment of the present invention. Referring now to Figure 6, a transceiver 600 includes a

transceiver port 602 for receiving and transmitting communication signals. In the described embodiment of the invention, transceiver port 602 receives signals transmitted at the RF and generates signals that are transmitted  
5 externally at the RF.

In addition to transceiver port 602, transceiver 600 further includes a plurality of RSSIs 606 and 608 that are for sensing the power level of the received signals and, more particularly, of the received signal as well as the received  
10 signal and interference. Transceiver 600 further includes a pair of low pass filters 614 and 616 and an automatic frequency control (AFC) circuit 620. Automatic frequency control 620 is for adjusting the LO frequency in the zero IF transceiver 600 to align with the desired frequency channel.  
15 In the described embodiment, AFC 620 adjusts the frequency of the LO frequency so that the received signal is located within the un-attenuated part of HP and LP filters. Transceiver 600 further comprises an A-D and D-A conversion circuitry 624 that is for converting signal formats as required. Additionally,  
20 transceiver 600 includes a base band processor 628 that is for processing the received signal and the signal to transmit. Transceiver 600 further includes up conversion circuitry 636 that receives signals that are to be transmitted at base band from base band processor 628 and then up converts the base

band signals to the RF for transmission from transceiver port 602. Finally, transceiver 600 includes down conversion circuitry 604 for converting a received RF signal to base band frequencies.

5 In operation, transceiver port 602 receives RF signals and converts the signals from the RF to base band. The down conversion is performed by down conversion circuitry 604 of Figure 6. Once the signal has been down converted, the RSSI filters 606 and 608 sense the power of the signal, as well as  
10 the signal plus interference, to determine the manner in which the amplification stages should be set for the received signal. While transceiver 600 shows a pair of low pass filters 614 and 616 which are used as a part of filtering higher frequency interference during the down conversion  
15 process as well as during the automatic frequency control or adjustment process by AFC 620, it is understood that transceiver 600 may include more than or less than two low pass filters. In general, low pass filters 614 and 616 represent the low pass filtering that occurs during the down-  
20 conversion process as well as during the automatic frequency control process to adjust the frequency of the received signals. Thus, in addition to sensing the power levels of the signal and interference of the received signal, the frequency is adjusted by AFC 620 at which time it is filtered by high



pass filter to remove DC offset and the  $1/f$  interference. After the low frequency interference has been removed, as well as the high frequency interference from the various filters, the signal is amplified and converted into digital domain for processing by the base band processor. The signal is amplified by LNA amp 610 and HP-VGA amps 612, whose total amplification is kept at a constant value (for a certain power level of received signal) but whose individual amplification is either increased or decreased according to the signal and signal plus interference ratios described earlier.

Figure 7 is a functional schematic diagram of a transceiver formed according to one embodiment of the present invention. Referring now to Figure 7, a transceiver system comprises radio circuitry 704 that is coupled to base band processing circuitry 708. The radio circuitry 704 performs filtering, amplification, frequency calibration (in part) and frequency conversion (down from the RF to base band and up from base band to the RF). Base band circuitry 708 performs the traditional digital signal processing in addition to partially performing the automatic frequency control. As may be seen, the single chip radio circuitry 704 is coupled to receive radio signals that are initially received by a transceiver and then converted by a Balun signal converter which performs single end to differential conversion for the

receiver (and differential to single end conversion for the transmitter end). The Balun are shown to be off chip in Figure 7, but they may be formed on chip with radio circuitry 704 as well.

5 More specifically, radio circuitry 704, and more particularly, portion 704A, includes a low noise amplifier 712 that is coupled to receive the RF from a transceiver port. The low noise amplifier 712 then produces an amplified signal to a mixer 716 that is for adjusting and mixing the RF as a part of the automatic frequency control that is performed by the radio and base band circuits 704 and 708. The outputs of the mixer (I and Q of a quadrature phase shift keyed signals) are then produced to a first HP-VGA stage 720.

10 The outputs of the first HP-VGA stage 720 are then produced to a first RSSI 728 as well as to a low pass filter stage 724. The outputs of the low pass filter stage 724 are then produced to a second RSSI 732, as well as to a second HP-VGA 736 and third HP-VGA 740 as may be seen in Figure 7.

15 In operation, the first RSSI measures the power level of the signal and interference. The second RSSI measures the power level of the signal only. The base band processing circuitry 708 then determines the ratio of the RSSI measured power levels to determine the relative gain level adjustments of the front and rear stage amplification stages. In the

described embodiment of the invention, if the power level of the signal and interference is approximately equal to or slightly greater than the power level of the signal alone, then the first amplification stages are set to a high value  
5 and the second amplification stages are set to a low value.

Conversely, if the power level of the signal and interference is significantly greater than the power of the signal alone, thereby indicating significant interference levels, the first amplification stages are lowered and the  
10 second amplification stages are increased proportionately.

Automatic frequency control circuit 704B includes low pass filters for filtering I and Q signals and mixer circuitry for actually adjusting LO frequency. The operation of mixers and phase locked loop for adjusting frequencies is known.  
15 Circuit 704B further includes JTAG (Joint Test Action Group, IEEE1149.1 boundary-scan standard) serial interface (SIO) circuitry 744 for transmitting control signals and information to circuit portions 704A (e.g., to control amplification levels) and to portion 704B (e.g., to control or specify the  
20 desired frequency for the automatic frequency control).

A portion of the automatic frequency control circuitry that determines the difference in frequency between a specified center channel frequency and an actual center channel frequency for a received RF signal is formed within

the base band circuitry in the described embodiment of the invention. This portion of the circuitry includes circuitry that coarsely measures the frequency difference and then uses measures the frequency difference in the digital domain to  
5 obtain a more precise measurement.

Finally, radio circuitry portion 704C includes low pass filtration circuitry for removing any interference that is present after base band processing as well as amplification, mixer and up converter circuitry for preparing a base band  
10 signal for transmission at the RF.

Figure 8 is a functional schematic diagram of an automatic frequency control (AFC) circuit formed according to one described embodiment of the invention. The AFC circuit of Figure 8 comprises a RF signal processing portion 804 and a  
15 base band signal processing portion 808. Generally, portion 804 is for adjusting LO frequency. Portion 808 is for determining the difference in center channel frequencies between the received RF and the expected frequency value for the received signal.

20 Analog-to-digital converters (ADC) 812 are used to convert the received analog signal into digital. ADC 812 is coupled to provide the received RF signal in a digital format to a frequency synchronization circuitry 820 that measures the frequency difference in a coarse degree of resolution. Digital

frequency control circuitry 816 performs its measurements and calibration in the digital domain and provides its results to frequency synchronization circuitry 820 to adjust the frequency difference of frequency synchronization circuit 820  
5 with a fine degree of resolution.

Frequency synchronization circuit 820, as a part of determining the difference in center channel frequency for the received signal and an expected value, receives and interprets a pilot signal that defines the expected center channel frequency. Accordingly, after measuring the actual center  
10 channel frequency of the received RF, frequency synchronization circuit 820 is able to determine the frequency difference. Frequency synchronization circuit 820 then produces a signal defining the difference in center channel  
15 frequency for the received signal and an expected value to signal generator 824. It is understood that the pilot channel is transmitted as a part of standard wireless network communication protocols for signal control and synchronization purposes.

20 Signal generator 824, upon receiving the difference in center channel frequency for the received signal and an expected value, produces quadrature phase shift keyed (I & Q) outputs for the received frequency difference to a pair of digital to analog converters (DAC) 828. The analog outputs of

DAC 828 are then passed to low pass filters 832 and are then up converted back to the RF. The I and Q RF signal components are then produced to mixer circuitry 836 that also receives a specified input from phase locked loop circuitry 840 to produce a received RF having a specified center channel frequency. It is understood that mixer circuitry 836 (including PLL circuitry 840) further receives control signals from base band processing circuitry (not shown in Figure 8) specifying the expected center channel frequency that is specified in the aforementioned pilot channel.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and detailed description. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but, on the contrary, the invention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the present invention as defined by the claims. As may be seen, the described embodiments may be modified in many different ways without departing from the scope or teachings of the invention.